Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-11 (canceled).

Claim 12 (currently amended): A processing system comprising:

a processor configured to

formulate an instruction and data, from a thread associated with a first context, for sending to a device, said instruction requesting the device to perform a command and write return data to a destination register associated with the first context in the processor;

perform a context switch to switch from processing the first context to a second context prior to receiving the return data; and

a bus controller configured to

generate a system bus operation to send the formulated instruction and data along with a thread identifier to the device.

Claim 13 (currently amended): The processing system of claim 12, wherein the processor is further configured to store an address of [[a]] the destination register ~~associated with the first context receiving the return data~~.

Claim 14 (original): The processing system of claim 13, wherein the bus controller is further configured to receive the device return data from a system bus along with the thread identifier.

Claim 15 (currently amended): The processing system of claim 14, wherein said processor is configured to

~~write the return data to the stored destination register associated with the first context; and~~

clear a wait bit in a status register associated with the first context after writing the return data to the destination register.

Claim 16 (original): The processing system of claim 12, wherein the device is a table lookup unit.

Claim 17 (original): The processing system of claim 12 said processor further including:

a context register file having a separate set of general registers for the first and second contexts; and

context control registers having a separate set of control registers for the first and second contexts.

Claim 18 (original): The processing system of claim 17, wherein the context register file includes 32 general registers for the each context.

Claim 19 (original): The processing system of claim 17, wherein the context register file includes for each context:

a context program counter;

a context status register; and

a write address register.

Claim 20 (original): The processing system of claim 19, wherein the context program counter holds a program counter pointing to a next instruction in an associated context.

Claim 21 (original): The processing system of claim 19, wherein the context status register holds data that indicates whether an associated context is awaiting data from an external source.

Claim 22 (currently amended): The processing system of claim 19, wherein the write address register stores an address of [[a]] the destination register ~~associated with a context awaiting data~~.

Claim 23 (original): The processing system of claim 19 further including:

a scheduler configured to select the second context to activate.

Claim 24 (original): The processing system of claim 23 further including

means for receiving an identifier of the second context to activate from the scheduler;

means for performing a next instruction in the first context; and

means for pointing a processor program counter to the context program counter in the context control register associated with the second context.

Claim 25-26 (canceled).

Claim 27 (currently amended): A method comprising:

formulating, in a processor, an instruction and data from a thread associated with a first context for sending to a device, the formulated instruction requesting the device to perform a command and write return data to a destination register associated with the first context in the processor;

performing, in the processor, a context switch to switch from processing the first context to a second context prior to receiving the return data; and

generating, in a bus controller, a system bus operation to send the formulated instruction and data along with a thread identifier to the device.

Claim 28 (currently amended): The method of claim 27 further comprising storing an address of [[a]] the destination register ~~associated with the first context for receiving the return data~~.

Claim 29 (currently amended): The method of claim 28 further comprising:

~~writing the return data to the destination register; and~~

clearing a wait bit in a status register associated with the first context after writing the return data to the destination register.

Claim 30 (previously presented): The method of claim 27 further comprising, in the device:

performing an operation in response to the formulated instruction and data; and

loading the return data resulting from the operation and thread identifier onto a system bus.

Claim 31 (previously presented): The method of claim 30 further comprising receiving the return data and thread identifier in the bus controller.

Claim 32 (previously presented): The method of claim 27 further comprising initiating the system bus operation in the processor before performing the context switch.

Claim 33 (previously presented): The method of claim 27 wherein performing the context switch comprises:

receiving an identifier of the second context;

performing a next instruction in the first context; and

changing a program counter in the processor from a value associated with the first context to a value associated with the second context.